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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,796	08/18/2003	Sheng-Tsai Chang	10894-US-PA	1795

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER
FARROKH, HASHEM

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,796	CHANG ET AL.	
	Examiner	Art Unit	
	Hashem Farrokh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,10-12 and 14* is/are rejected.

7)☒ Claim(s) *5-9 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The instant application having application No. 10/604,796 has a total of 14 claims pending in the application; there are 2 independent claims and 12 dependent claims, all of which are ready for examination by the examiner.

INFORMATION CONCERNING CLAIMS:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2,11-12, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,240,504 B1 to Boutaud et al. (hereinafter Boutaud).

1. In regard to claim 1, Boutaud teaches:

"A device **(e.g., see Figs.1A-1B)** for extending address space by inserting a waiting state, **(e.g., see abstract; column 2, lines 66-67; column 3, lines 1-9)** wherein the device is coupled to an external memory through a bus, **(e.g., see column 27, lines 41-42; column 39, lines 52-53; elements 25 and 61 in Fig. 1; elements 951 and 959 in Fig. 26)** and the external memory has stored at least a first program, **(e.g., see column 1, lines 44-49)** the device comprising:" *Boutaud teaches that ROM can be used in either on or off the microcontroller or*

microcomputer device. Fig. 26 shows that the device is coupled to the external memories (both RAM and ROM).

"a read-only memory (ROM), for storing a second program;" **(e.g., see column 1, line 51; column 35, lines 33-35; column 36, lines 42-43; element 61 in Figs. 1a and 21).**

"a central processing unit (CPU), coupled to the ROM, for executing the first program or the second program;" **(e.g., see column 36, lines 34-45; elements 13, 15, and 61).** *Fig. 21 shows that CPU is coupled to the program memory or ROM (element 61).*

"and a memory interface controller, for inserting a waiting state into the CPU when the CPU intends to execute an instruction of the first program stored in the external memory." **(e.g., see column 39, lines 62-67; column 40, lines 1-6 and 40-45; Fig. 26-27).**

2. In regard to claims 2 and 12, Boutaud teaches:

"wherein the device is a micro-controller." **(e.g., see column 3, lines 23-26; Figs. 1A-1B).**

3. In regard to claim 11, Boutaud teaches:

"An operation method on a device for extending address space by inserting a waiting state, wherein the device at least includes a central processing unit (CPU),

the operation method comprising:" **(e.g., see column 39, lines 62-67; column 40, lines 1-6 and 40-45; Fig. 26-27).**

"setting a predetermined address range;" **(e.g., see column 2, lines 61-67; column 3, lines 1-9).** *For example the programming register is programmed or set with a value representative of wait-state of the corresponding address ranges of the peripheral device (e.g., memory such as ROM).*

"judging whether or not an address of a program instruction to be fetched is located within the predetermined address range; "**(e.g., see column 40, lines 40-45 and 65-67; Fig. 27).** *Judging or determination is done based on Type of peripheral or memory devices. Based on this determination registers 975 shown in Fig. 27 is programmed to provide 0-15 wait-states.*

"inserting a waiting state into the CPU when the address is located out of the predetermined address range, until the program instruction is completely fetched;" **(e.g., see column 39, lines 64-67; column 40, lines 45-48).** *For example a predetermined number of wait-state based on the peripheral devices (including memory) programmed into the programmable registers. The number of wait-states can be further adjusted or extended based upon the state of ready signal* $\overline{RDY}$.

"and executing the program instruction by the CPU." **(e.g., see column 27, lines 35-42; column 39, lines 64-67).** *The ROM is being accessed to down load the program for inherent execution.*

4. In regard to claim 14, Boutaud teaches:

"wherein predetermined address range can be freely set." **(e.g., see column 40, lines 26-28; Fig. 27).** *For example the processor can freely set the predetermined address range by programming the programmable registers (element 975 in Fig. 27).*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-4 and 10 rejected under 35 U.S.C. 103(a) as being unpatentable over boutaud in view of U.S. Patent 5,668,971 to Neufeld.

5. In regard to claim 3, Boutaud further teaches:

"wherein the memory interface controller **(e.g., see abstract; column 27, lines 35-42; element 41 in Fig. 1b**) comprises: a memory interface **(e.g., see column 40, lines 10-11)**, coupled the bus, **(e.g., see element 111D in Fig. 1b; element 957 in Fig. 26)** serving as a transmission interface between the memory interface controller and the bus;" **(e.g., see column 39, lines 52-61; Fig. 26).** *For example Fig. 26 shows that processor 11 coupled to the external peripheral devices (e.g., memory). Fig. 1b a peripheral controller (element 41 coupled to the data bus).*

"and a state control unit, **(e.g., see element 971 in Fig. 27**) coupled to the memory interface, **(e.g., see element 959 in Figs. 26-27**) the range checking unit, **(e.g., see element 977 in Fig. 27)** and the CPU, **(e.g., see element 11 in Fig. 26)** used for inserting the waiting state into the CPU when the range checking signal is received." **(e.g., see column 40, lines 26-31; column 41, lines 1-12; Figs. 26-27).** *For example the programmable decoder decodes the three most significant bits of peripheral devices' addresses that are within the its decoding range and enables one of the eight registers 975 shown in Fig. 27 to be programmed. One of the registers is being selected and provides a number of wait values for the wait state generator (element 971 in Fig.27). The output of the wait state generator along with* $\overline{RDY}$ *signal are fed to the two inputs OR GATE 974 that generate the* $\overline{WAIT}$ *signal (e.g., wait state).*

"a range checking unit, **(e.g., see elements 971 and 975 in Fig. 27**) used to judge whether or not an address of an information, **(e.g., see elements 959 and MSB in Fig. 27**) which is to be accessed by the CPU, **(e.g., see element 11 Fig. 26**) is located within a predetermined range, **(e.g., see column 40, lines 56-67; column 41, lines 1-12; Figs. 26-27**). *However,* Boutaud does not expressly teach: "selectively issuing a range checking signal;"

Neufeld teaches: "selectively issuing a range checking signal;" **(e.g., see column 4, lines 19-23; column 18, lines 13-23; element INRNG* in Fig. 9**) *for generating or issuing the range checking signal INRNG* to indicate that the processor address is within the protected boundary address range stored in latches.*

Disclosures by boutaud and Neufeld *are analogous because both references teach methods of accessing the external memory and inserting wait state when the access time of the external memory is greater than operating speed of the processor.*

At the time of invention it would have been obvious to a person of ordinary skill in art to modify the data processing device of boutaud *to include the circuitry to generate or issue the address range checking signal taught by* Neufeld.

The motivation for doing so, as taught by column 23, lines 46-48 of Neufeld, *is to avoid problems associated with latency and memory refresh.*

Therefore, it would have been obvious to combine the teaching of Neufeld *with* Boutaud for benefit of avoiding the problems associated with latency *to obtain the invention as specified in the claim.*

6. In regard to claim 4, Neufeld teaches:

"wherein the range checking unit issues the range checking signal when the address of the information to be accessed by the CPU is located within an address range of the external memory or out of an address range of the ROM." **(e.g., see column 4, lines 19-23; column 18, lines 13-23; element INRNG* in Fig. 9**). *When INRNG* is active state, it indicates that address of the information to be accessed by the CPU is located within an address range of the external memory.*

7. In regard to claim 10, Boutaud teaches:

"wherein predetermined address range can be freely set." **(e.g., see column 40, lines 26-28; Fig. 27).** *For example the processor can freely set the predetermined address range by programming the programmable registers (element 975 in Fig. 27).*

ALLOWABLE SUBJECT MATTER

Claims 5-9 and 13 are objected to as being dependent upon rejected based claims, but would be allowable if rewritten in correct and independent form including all of the limitations of the base claim and any intervening claims.

1. The primary reason for allowance of claims 5-8 in instant application is the combination with the inclusion of the following limitations: **a ready flag, coupled to the buffer and the CPU, wherein the CPU inquires the ready flag, and the CPU correctly accesses the information through the buffer when buffer has correctly accessed the information of the external memory through the memory interface.**

2. The primary reason for allowance of claims 9 in instant application is the combination with the inclusion of the following limitations: **wherein a transmission unit in one time is one bit, two bits, one nibble, or one byte.**

3. The primary reason for allowance of claims 13 in instant application is the combination with the inclusion of the following limitations: **wherein the waiting state being inserted into the CPU cause a clock state of the CPU to remain.**

: IMPORTANT NOTE :

I f the applicant should choose to rewrite the independent claims to include the limitations recited in either one of the claims, the applicant is encouraged to ***amend the title of the invention*** *such that it is descriptive of the invention as claimed as required be sec.* ***606.01*** *of the* ***MPEP****. Furthermore, the* ***summary of invention*** *and the* ***abstract*** *should be amended to bring them into harmony with the allowed claims as required by paragraph 2 of* ***sec. 1302.01*** *of the* ***MPEP****.*

As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not compiled with. See ***37 C.F.R. § 1.111(b)*** *and* ***§ 707.07(a) of the M.P.E.P.***

Conclusion

The prior art made of record and not relied upon are as follows:

1. U. S. Patent No. 6,343,353 to Kim describes Micro-controller unit for accessing external memory using microcode.

2. U. S. Patent No. 5,329,621 to Burgesset al. describes Microprocessor which optimizes bus utilization based upon bus speed.

3. U. S. Patent No. 5,465,343 to Henson et al. describes Shared memory array for data block and control program storage in disk drive.

4. U. S. Patent Publication No. 2003/0233527 to Kawasaki et al. describes Single-chip microcomputer.

Any inquiry concerning this communication should be directed to Hashem Farrokh whose telephone number is (571) 272-4193. The examiner can normally be reached Monday-Friday from **8:00 AM to 5:00 PM.**

If attempt to reach the above noted Examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Donald A Sparks, can be reached on (571) 272-4201. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either private PAIR or Public PAIR. Status information for unpublished application is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBS) at 866-217-9197 (toll-free).

HF.
HF

2005-07-30

DONALD SPARKS
SUPERVISORY PATENT EXAMINER